A Novel Bipolar-MOSFET Low-Noise Amplifier (BiFET LNA), Circuit Configuration, Design Methodology, and Chip Implementation

Pingxi Ma, *Member, IEEE*, Marco Racanelli, *Member, IEEE*, Jie Zheng, *Member, IEEE*, and Marion Knight

***Abstract*—This paper proposes a new RF circuit configuration: the Bipolar cascoded with a mosFET (BiFET). Applying the BiFET for low-noise amplifiers (LNAs), we have developed a new BiFET-based design methodology. By using this methodology, a BiFET LNA has been designed based on Jazz Semiconductor Inc.'s SiGe90 BiCMOS process. The packaged chip tested on board has demonstrated a 16-dB power-gain 1.6-dB noise-figure −6.5-dBm input third intercept point while consuming only 3 mW (2.2 V × 1.4 mA) in the personal communication system (PCS) band. To our knowledge, this is the lowest current silicon-based LNA reported to date that maintains good PCS band performance.**

***Index Terms*—Bipolar, bipolar cascoded with a mosFET (BiFET), low-noise amplifier (LNA), MOSFET.**

I. Introduction

THE low-noise amplifier (LNA) is a key component of wireless communication systems. The LNA specification, high gain, and low-noise figure can significantly improve the system noise performance, while high linearity can effectively reduce adjacent channel interference and transmitter desensitization. Since receivers have to be continuously powered to explore pilot signal, dc-bias current is a critical specification for the LNA design. A large dc-bias current can increase circuit power consumption and degrade the battery life.

In order to obtain high gain, high linearity, low noise figure, and low bias current, there are a variety of LNA configurations in use. As Fig. 1(a)–(c) shows, six existing configurations of the LNA can be identified as either bipolar or MOSFET with single-device, cascade, or cascode architecture, respectively. The single-device LNA generally has a lower power gain than the cascaded LNA, but consume less power. The cascoded LNA has been used to maintain low power consumption and higher gain with higher reverse isolation simultaneously. Implementations that use only bipolar devices typically have better noise figure, while implementations that use MOS devices can achieve higher linearity. This is due to the inherent properties of the bipolar and MOS device.

The modern SiGe BiCMOS process has merged the bipolar device and MOSFET into the same technological platform [1], [2]. While BiCMOS logic cells have been proposed previously to take advantages of the bipolar and MOSFET devices [3], no equivalent for RF circuit blocks has yet been presented. In this paper, we report a novel configuration of a bipolar cascoded with mosFET (BiFET) and use it for an LNA design, as shown in Fig. 1(d). Such an approach combines a very low-noise bipolar first stage with a linear cascoded MOSFET (BiFET) to improve the tradeoff between power consumption, noise, gain, and linearity relative to the more traditional configurations shown in Fig. 1(a)–(c). In Section II, we develop a new BiFET-based analytical theory on gain, noise figure, and linearity. In Section III, we present a design methodology using the newly developed theory. In Section IV, we demonstrate a chip implementation and, in Section V, we present a conclusion.

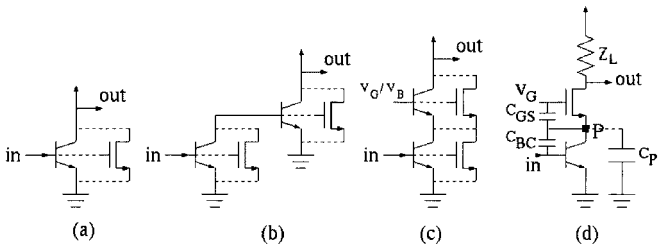

Fig. 1. LNA circuit configurations. (a) Single-device, (b) cascade, and (c) cascode with a Bipolar and MOSFET, respectively. (d) BiFET LNA with Bipolar cascoded with a MOSFET.

II. Analytical Theory

A. Voltage Gain

Fig. 1(d) shows the newly proposed configuration. The bipolar is cascoded with a MOSFET loading impedance Z_L. The capacitance at node P is marked as C_P and it can be expressed as a function of $C_{\rm GS}$ and $C_{\rm BC}$ (see the Appendix). Using the small-signal frequency response, we can obtain a voltage gain as [4]

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = -g_{\rm mBip} Z_L \cdot \frac{\eta}{(\eta+1)} \tag{1}$$

where $\eta = g_{\rm mMOS}/C_P s$, $g_{\rm mBip}$, and $g_{\rm mMOS}$ is the bipolar and MOSFET transconductance, respectively. For a large $g_{\rm mMOS}$, $\eta \gg 1$, (1) can be reduced to

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = A_{\rm cascode} = -g_{\rm mBip} Z_L \tag{2}$$

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The authors are with Jazz Semiconductor Inc., Newport Beach, CA 92660 USA (e-mail: pingxi.ma@jazzsemi.com; marco.racanelli@jazzsemi.com; jie.zheng@jazzsemi.com; marrion.knight@jazzsemi.com).

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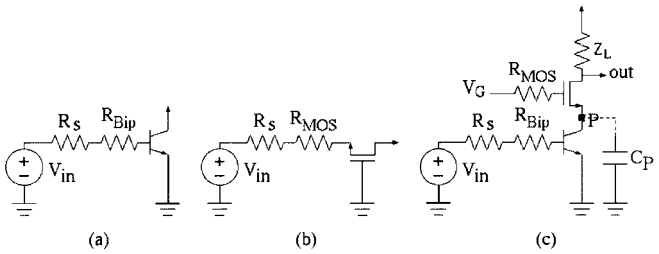

Fig. 2. Equivalent circuits for noise-figure calculation in: (a) common-emitter, (b) common-gate, and (c) BiFET configurations.

where A_{cascode} is the voltage gain achieved with the BiFET operating in the cascode mode. For a smaller g_{mMOS}, $\eta \ll 1$, (1) can be reduced to

$$\begin{aligned}\frac{V_{\text{out}}}{V_{\text{in}}}(s) &= A_{\text{cascade}} \\ &= \left(-g_{\text{mBip}} \cdot \frac{1}{C_P s}\right) \cdot (g_{\text{mMOS}} \cdot Z_L) \\ &= A_{\text{Bip}} \cdot A_{\text{MOS}} \end{aligned} \tag{3}$$

where A_{cascade} is the voltage gain achieved with the BiFET operating in the cascade mode. A_{Bip} and A_{MOS} are the voltage gain for the bipolar and MOSFET stages, respectively. In the actual application, the LNA operates between the cascode and cascade modes of operation.

B. Noise Figure

The noise figure of circuit can be expressed as [4]

$$\text{NF} = 1 + \frac{\overline{V}_n^2}{4kTR_s\Delta f} + \frac{\overline{I}_n^2}{4kT \cdot \frac{1}{R_s} \cdot \Delta f} \tag{4}$$

where $\overline{V}_n^2$ and $\overline{I}_n^2$ are the input-referred voltage and current noise sources, respectively. R_s is the source resistance, and Δf is the frequency bandwidth.

For the common-emitter HBT used in the BiFET LNA, the base resistance r_b of the HBT should be low to achieve a lower noise figure. The current noise source $\overline{I}_n^2$ could be neglected in this case. The noise figure in Fig. 2(a) can be written as

$$\text{NF}_{\text{Bip}} = 1 + \frac{R_{\text{Bip}}}{R_s} \tag{5a}$$

with

$$R_{\text{Bip}} = r_b + \frac{1}{2g_{\text{mBip}}} \tag{5b}$$

where R_{Bip} is the equivalent noise resistance of the HBT.

For a common-gate MOSFET, the current noise source $\overline{I}_n^2$ could be neglected due to the large output impedance [4]. The noise figure in Fig. 2(b) can be written as

$$\text{NF}_{\text{MOS}} = 1 + \frac{R_{\text{MOS}}}{R_s} \tag{6a}$$

with

$$R_{\text{MOS}} = r_g + \frac{1}{2g_{\text{mMOS}}} \tag{6b}$$

where R_{MOS} is the equivalent noise resistance and r_g is the gate resistance.

The BiFET LNA noise figure can be calculated by using Fig. 2(c). There are two noise contributions, i.e., R_{Bip} and R_{MOS}, to the total noise figure. The R_{MOS} contribution can be calculated based on voltage gains between V_G and V_{out} and V_{in} and V_{out}. The R_{MOS} contribution to the "out" terminal can be expressed as

$$\overline{V}_{n,\text{out},R_{\text{MOS}}}^2 = \left(\frac{V_{\text{out}}}{V_G}\right)^2 \cdot \overline{V}_{n,R_{\text{MOS}}}^2 \tag{7a}$$

where the voltage gain is [4]

$$\frac{V_{\text{out}}}{V_G} = \frac{Z_L}{g_{\text{mMOS}}^{-1} + (C_P s)^{-1}} \tag{7b}$$

and the noise voltage is

$$\overline{V}_{n,R_{\text{MOS}}}^2 = 4kTR_{\text{MOS}}\Delta f. \tag{7c}$$

The input-referred noise voltage resulting from R_{MOS} can be written as

$$\overline{V}_{n,\text{in},R_{\text{MOS}}}^2 = \left(\frac{V_{\text{in}}}{V_{\text{out}}}\right)^2 \cdot \overline{V}_{n,\text{out},R_{\text{MOS}}}^2. \tag{8}$$

The input-referred noise voltage resulting from R_{Bip} can be written as

$$\overline{V}_{n,\text{in},R_{\text{Bip}}}^2 = 4kTR_{\text{Bip}}\Delta f. \tag{9}$$

Since the noise source R_{MOS} is not correlated with R_{Bip}, the total input-referred noise voltage can be obtained as

$$\overline{V}_{n,\text{in}}^2 = \overline{V}_{n,\text{in},R_{\text{MOS}}}^2 + \overline{V}_{n,\text{in},R_{\text{Bip}}}^2. \tag{10}$$

Substituting (10) into (4) and assuming $\overline{I}_n^2 = 0$, we can express the total noise figure as a function of NF_{Bip} and NF_{MOS} through the corresponding equations as follows:

$$\text{NF} - 1 = (\text{NF}_{\text{Bip}} - 1) + \frac{1}{A_{\text{Bip}}^2}(\text{NF}_{\text{MOS}} - 1). \tag{11}$$

This equation is presented here for the first time. It clarifies that the cascode noise figure is mainly determined by the input transistor rather than the cascoded device. The smaller the capacitance (C_P) at node P is, the higher the voltage gain (A_{Bip}) is, which reduces the cascoded MOSFET's noise and totally achieves a lower noise figure.

C. Input Third Intercept Point (IIP_3)

The input–output relationship of a memoryless nonlinear system can be approximated with a polynomial [5]

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots. \tag{12}$$

The IIP3 should be

$$\text{IIP}_3 = \sqrt{\frac{4}{3} \cdot \left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{13}$$

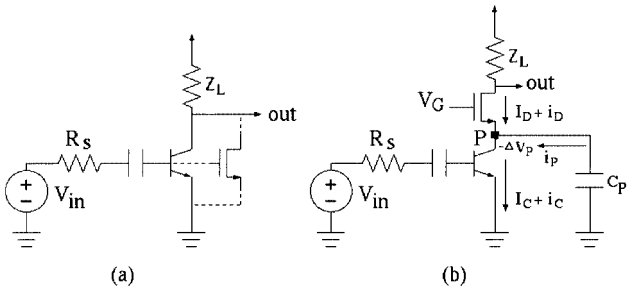

Fig. 3. Equivalent circuits for the IIP_3 calculation in bipolar/MOSFET: (a) single-device and (b) BiFET configurations.

For the input bipolar transistor, the input–output relationship in Fig. 3(a) can be obtained as

$$\begin{aligned} I_C &= I_S \exp\left(\frac{V_{\mathrm{BEO}}+V_{\mathrm{in}}}{V_T}\right) \\ &= I_S \exp\left(\frac{V_{\mathrm{BEO}}}{V_T}\right) \\ &\quad \cdot \left[1+\frac{V_{\mathrm{in}}}{V_T}+\frac{1}{2}\left(\frac{V_{\mathrm{in}}}{V_T}\right)^2+\frac{1}{6}\left(\frac{V_{\mathrm{in}}}{V_T}\right)^3+\cdots\right] \end{aligned} \tag{14}$$

where I_C is the collector current, I_S is the reverse saturation current, V_{BEO} is the emitter–base dc-bias voltage, V_{in} is the input signal, and V_T is the thermal voltage. The IIP_3 can be obtained by using (13)

$$\mathrm{IIP}_{3\mathrm{Bip}} = 2\sqrt{2}\cdot V_T. \tag{15}$$

Substituting the bipolar transistor in Fig. 3(a) for the cascoded MOSFET, we can achieve a larger IIP3 and further assume it to be infinite due to the MOSFET's square *I–V* law.

The BiFET's IIP3 can be calculated in Fig. 3(b). We can obtain a group of equations as

$$I_D = M(-V_{PG}-V_{\mathrm{Th}})^2 \tag{16a}$$

$$I_D + i_D = M(-V_{PG}-\Delta v_P - V_{\mathrm{Th}})^2 \tag{16b}$$

$$i_P = \Delta v_P C_P s \tag{16c}$$

$$i_C = I_S \exp\left(\frac{V_{\mathrm{in}}}{V_T}\right) \tag{16d}$$

$$i_D = i_C - i_P \tag{16e}$$

with $M = (1/2)\,\mu_n C_{\mathrm{ox}}(W/L)$, where μ_n is the electron mobility, C_{ox} is the gate–oxide capacitance density, and W and L is the gatewidth and gate length, respectively. Substituting (16a) and (16c) into (16b), we can get

$$i_D = M\Delta v_P^2 - g_{\mathrm{mMOS}}\cdot\Delta v_P \tag{16f}$$

with

$$g_{\mathrm{mMOS}} = 2M(-V_{PG}-V_{\mathrm{Th}}). \tag{16g}$$

Substituting (16c) and (16f) into (16e), we obtain

$$\Delta v_P^2 - \frac{g_{\mathrm{mMOS}}-C_P s}{M}\cdot\Delta v_P = \frac{i_C}{M}. \tag{16h}$$

Solving (16h), we can obtain a solution of Δv_p

$$\Delta v_P = -\sqrt{\frac{i_C}{M}+\frac{(g_{\mathrm{mMOS}}-C_P s)^2}{4M^2}}+\frac{g_{\mathrm{mMOS}}-C_P s}{2M}. \tag{16i}$$

The output current i_D can be rewritten as

$$\begin{aligned} i_D &= I_S \exp\left(\frac{V_{\mathrm{in}}}{V_T}\right) - C_P s \\ &\quad \cdot \left[-\sqrt{\frac{I_S}{M}\exp\left(\frac{V_{\mathrm{in}}}{V_T}\right)+\frac{(g_{\mathrm{mMOS}}-C_P s)^2}{4M^2}}\right. \\ &\quad \left. +\frac{g_{\mathrm{mMOS}}-C_P s)}{2M}\right]. \end{aligned} \tag{16j}$$

The IIP_3 can be derived by using (16j) with i_D being a function of V_{in}.

III. Design Methodology

A. Design Guideline

We can rewrite the normalized voltage gain in (1) as a function of η

$$G_{\mathrm{NORM}} = \frac{\eta}{(\eta+1)} \tag{17a}$$

with

$$G_{\mathrm{NORM}} = \frac{V_{\mathrm{out}}}{A_{\mathrm{cascode}}V_{\mathrm{in}}}. \tag{17b}$$

The normalized noise figure can be a function of η through (11)

$$\mathrm{NF}_{\mathrm{NORM}} = \frac{1}{\eta^2} \tag{18a}$$

with

$$\mathrm{NF}_{\mathrm{NORM}} = \frac{3}{4g_m(\mathrm{ratio})}\cdot\left(\frac{\mathrm{NF}-1}{\mathrm{NF}_{\mathrm{Bip}}-1}-1\right) \tag{18b}$$

and

$$g_m(\mathrm{ratio}) = \frac{g_{\mathrm{mMOS}}}{g_{\mathrm{mBip}}}\cdot\frac{1+1.5g_{\mathrm{mMOS}}r_g}{1+2g_{\mathrm{mBip}}r_b}. \tag{18c}$$

The input–output relationship in (16j) can be a function of η as follows:

$$\begin{aligned} i_D &= I_S \exp\left(\frac{V_{\mathrm{in}}}{V_T}\right) - C_P s \\ &\quad \cdot \left[-\sqrt{\frac{I_S}{M}\exp\left(\frac{V_{\mathrm{in}}}{V_T}\right)+\frac{C_P^2 s^2(\eta-1)^2}{4M^2}}+\frac{C_P s(\eta-1)}{2M}\right] \end{aligned} \tag{19}$$

when $\eta \ll 1$ or $g_{\mathrm{mMOS}} \ll C_p s$, the node P in Fig. 3(b) is ac shorted to ground, no signal is output, and (19) is reduced and tends to $i_D = 0$, which causes a large IIP_3. When $\eta \gg 1$ or $g_{\mathrm{mMOS}} \gg C_p s$, the node P is open and (19) is reduced to $i_D = I_s \exp(V_{\mathrm{in}}/V_T)$, which causes IIP_3 to equal that of the bipolar single device. The normalized IIP_3 is

$$\mathrm{IIP}_{3\mathrm{NORM}} = \frac{\mathrm{IIP}_3}{\mathrm{IIP}_{3\mathrm{Bip}}} = 1 \tag{20}$$

when $\eta \approx 1$ or $g_{\mathrm{mMOS}} \approx C_p s$, (19) can be reduced to

$$i_D = I_S \exp\left(\frac{V_{\mathrm{in}}}{V_T}\right)+\frac{C_P s}{\sqrt{M}}\exp\left(\frac{V_{\mathrm{in}}}{2V_T}\right). \tag{21}$$

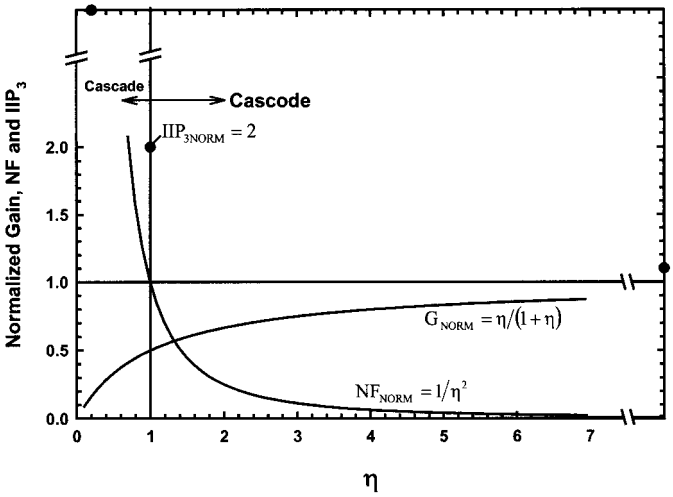

Fig. 4. Normalized LNA specifications analyzed with η for the design methodology development.

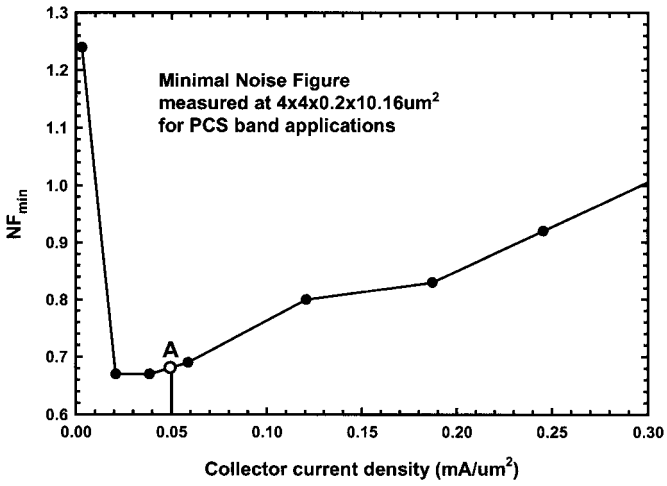

Fig. 5. Measured minimal noise figure versus collector current density based on Jazz Semiconductor Inc.'s SiGe90 process.

We can write the polynomial of (21) as

$$i_D = I_S + \frac{C_P s}{\sqrt{M}} + \left(I_S + \frac{C_P s}{2\sqrt{M}}\right)\left(\frac{V_{\text{in}}}{V_T}\right) + \frac{1}{2}\left(I_S + \frac{C_P s}{4\sqrt{M}}\right) \times \left(\frac{V_{\text{in}}}{V_T}\right)^2 + \frac{1}{6}\left(I_S + \frac{C_P s}{8\sqrt{M}}\right)\left(\frac{V_{\text{in}}}{V_T}\right)^3 + \cdots. \quad (22)$$

IIP_3 can be obtained through (13)

$$\text{IIP}_3 = 2\sqrt{2}V_T \cdot \sqrt{\frac{I_s + \frac{C_P s}{2\sqrt{M}}}{I_S + \frac{C_P s}{8\sqrt{M}}}}. \quad (23)$$

Since $I_C = I_D$, $((C_p s)/\sqrt{M}) = ((g_{\text{mMOS}})/\sqrt{M}) = 2\sqrt{I_C}$, and $\sqrt{I_C} \gg 4I_s$, the normalized IIP_3 can be expressed by using (15)

$$\text{IIP}_{3\text{NORM}} = \frac{\text{IIP}_3}{\text{IIP}_{3\text{Bip}}} = 2. \quad (24)$$

Fig. 4 shows the normalized gain, noise figure, and IIP_3 varying with η through (17a), (18a), (20), and (24). When $\eta \ll 1$, even though we could achieve good linearity, low gain and high noise figure are not desirable. When $\eta \gg 1$, both the noise and gain can achieve good performance. However, a large current is required, degrading power consumption. When $\eta \approx 1$, the achievable noise is nearly the same as that achieved with the bipolar single device since $g_m(\text{ratio}) \ll 1$. With $\eta \approx 1$, the gain is half of A_{cascode}, since A_{cascode} is generally at least a double of the bipolar single-device gain, we could still achieve nearly the same gain as we could with the bipolar single device. Linearity, however, is twice what is achievable in the bipolar single device, as measured by IIP_3. Therefore, $\eta \approx 1$ represents an optimum choice for designing and biasing the BiFET LNA.

B. Design Procedure

The BiFET LNA design could start with the input bipolar transistor. The circuit should be biased near the minimal noise-figure valley, as shown in Fig. 5. An acceptable biasing current could be determined by using $A_E \times J_C$ (at "A"), where A_E is the emitter area and J_C is the collector current density.

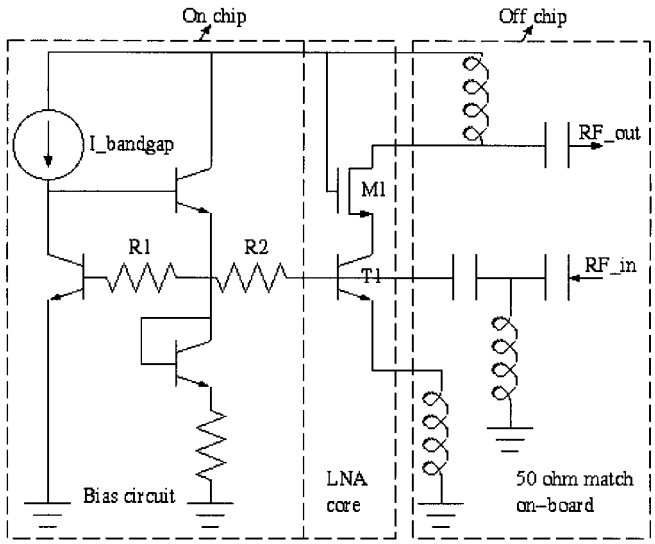

Fig. 6. Simplified BiFET LNA schematic in implementation.

The next step is to choose a matching MOSFET based on $\eta \approx 1$ or $g_{\text{mMOS}} \approx C_p s$ to optimize the design specification. C_P in (A.4) can be reduced by assuming $g_{\text{mBip}} \gg g_{\text{mMOS}}$ and $((g_{\text{mBip}})/(C_{\text{BC}} s)) \gg 1$ as (shown in the Appendix)

$$C_P = C_{\text{BC}} + C_{\text{GS}}. \quad (25)$$

Since $g_{\text{mMOS}} = 2\sqrt{MI_D} = 2\sqrt{MI_C}$ and $C_{\text{GS}} \approx (2/3)\, WLC_{\text{ox}}$ in the saturation region, we can obtain an equation of W through $\eta = 1$ as follows:

$$\left(\sqrt{W}\right)^2 - \frac{1}{2\pi}\sqrt{\frac{9I_C\mu_n}{2C_{\text{ox}}L^3 f_0^2}} \cdot \sqrt{W} = -\frac{3C_{\text{BC}}}{2LC_{\text{ox}}} \quad (26)$$

where f_0 is the operation frequency of the LNA. Solving (26), we can derive

$$W = \left(\frac{1}{2\pi}\sqrt{\frac{9I_C\mu_n}{8C_{\text{ox}}L^3 f_0^2}} + \frac{1}{2\pi}\sqrt{\frac{9I_C\mu_n}{8C_{\text{ox}}L^3 f_0^2} - \frac{3C_{\text{BC}}}{2C_{\text{ox}}L}}\right)^2 \quad (27)$$

TABLE I
BiFET LNA PERFORMANCE MEASURED AT THE PCS BAND (1.96 GHz)

Supply	Power Gain	Noise Figure	IIP3	$\|S_{11}\|$	$\|S_{22}\|$	$\|S_{12}\|$	Current
2.2V	16.0dB	1.6dB	-6.5dBm	-10.8dB	-14.5dB	-28.0dB	1.43mA
3.0V	20.3dB	1.3dB	-6.0dBm	-10.4dB	-13.2dB	-28.2dB	3.0mA
5.0V	19.5dB	1.55dB	-1.0dBm	-10.2dB	-12.7dB	-28.5dB	3.5mA

TABLE II
VALUES OF η IN THE BiFET LNA IMPLEMENTATION

Supply	g_{mBip}	g_{mMOS}	C_{GS}	C_{BC}	η
2.2V	50.5mS	6.8mS	0.25pF	0.11pF	1.53
3.0V	105.9mS	9.1mS	0.25pF	0.11pF	2.05
5.0V	122.5mS	10.2mS	0.25pF	0.11pF	2.30

where f_0 must satisfy

$$f_0 \leq \frac{1}{2\pi}\sqrt{\frac{3I_C\mu_n}{4C_{\rm BC}L^2}}. \tag{28}$$

Equation (28) gives the highest operation frequency limit of the BiFET LNA. The high bias current, low B–C capacitance and short-channel length MOSFET is essential to achieving a higher operation frequency. Using (27), we can calculate a W based on a given L as an initial value for the design simulation. By repeating the above procedure and adding proper simulation optimization, we can achieve good performance and satisfy the design specification.

IV. CHIP IMPLEMENTATION

The BiFET LNA is designed using Jazz Semiconductor Inc.'s 0.18-μm SiGe90 process. This technology offers two types of SiGe n-p-n's: a 75-GHz f_T, 130-GHz $f_{\rm MAX}$, 3.8-V $\rm BV_{CEO}$ high-speed device, and a 35-GHz f_T, 100-GHz $f_{\rm MAX}$, 6-V $\rm BV_{CEO}$ high-voltage device. It also offers poly resistors, 3.3-V CMOS, high-Q metal–insulator–metal (MIM) capacitors, and high-Q inductors. The process used includes a 3-μm-thick top-metal inductor built on an 8 $\Omega\cdot$ cm silicon substrate. More details on the technology can be found in [1] and [2].

The BiFET LNA includes the LNA core, bandgap-referenced circuit, and input and output 50-Ω on-board match. In Fig. 6, the bipolar transistor $T1$ and MOSFET $M1$ have been designed by using the methodology proposed in Section III. We consider $T1$ first. As Fig. 5 shows, the minimal noise figure can be achieved by biasing the transistor at a current density $J_C \approx 0.05$ mA/μm^2. The emitter area can be obtained based on the current specification $I_C \approx 1.5$ mA, i.e., $A_E = 30\ \mu$m^2. Thus, we use four parallel n-p-n's with each of them having four emitter fingers, five base fingers, and two collector fingers. The total emitter area is $0.2 \times 10.16 \times 4 \times 4 \approx 32.5\ \mu$m^2 close to the desired 30 μm^2. The next step is to design MOSFET $M1$. We firstly determine whether the personal communication system (PCS) band frequency is over the maximum operation frequency predicted by (28). Even though the process offers MOSFETs with a shortest gate length $L = 0.35\ \mu$m, we still use a longer gate $L = 0.8\ \mu$m in the BiFET LNA design to more efficiently verify the design methodology. If we could achieve good performance by using $L = 0.8\ \mu$m, the shorter gate length should have no problem performing well. Considering a typical electron mobility $\mu_n = 260\ \text{cm}^2/V\cdot s$, we can obtain the maximal operation frequency $f_0 = 3.2$ GHz, which satisfies the PCS band specification. With a typical 20-Å gate oxide and the 0.8-μm gate length, we can calculate the gatewidth of $W \approx 100\ \mu$m using (27). Taking the MOSFET with $L = 0.8\ \mu$m and $W = 10\ \mu$m and using ten fingers (100 μm) as an initial value, we have optimized the BiFET LNA simulation and determined an eight-finger MOSFET to be the final choice.

The fabricated BiFET LNA is packaged in a 32-pin land grid array (LGA). A die photograph is shown in [6]. We have performed room-temperature tests with a supply voltage ranging from 2.2 to 5 V. Table I shows a typical measurement result at a frequency of 1.96 GHz. The LNA achieves 16-dB power gain, -6.5-dBm $\rm IIP_3$, and 1.43-mA/3.1-mW power consumption at 2.2-V supply voltage. When biased to 3 and 5 V, the LNA achieves a higher power gain (20.3 dB at 3 V), higher $\rm IIP_3$ (-6 dBm at 3 V), and lower noise figure (1.3 dB at 3 V). With all the bias conditions, the LNA also achieves a higher reverse isolation ($\sim$28 dB) than the single-device LNA ($\geq$20 dB). To our knowledge, the BiFET LNA configuration and design methodology has resulted in the lowest power consumption reported to date [7], [8].

The design methodology can also be verified by identifying the η value at different supply voltages. Table II shows the calculated η value based on the simulation modeling parameter. At 2.2 V and 1.43 mA, we get $\eta = 1.53$, which is close to $\eta = 1$, the design optimized point in the design methodology. The power gain of 16 dB is equivalent to the bipolar single-device LNA result as the design methodology predicts. When the bias is 3

and 5 V and the current is higher, the increased g_{mMOS} makes η increase to around two, but still not far from $\eta = 1$. These evidence that $\eta \approx 1$ should be an optimized point for the BiFET LNA design.

V. Conclusion

This paper has proposed a new RF circuit configuration: the BiFET LNA, which is based on Jazz Semiconductor Inc.'s SiGe90 BiCMOS process. This LNA merges the low-noise advantage of SiGe bipolar devices with the inherent linearity advantages of MOSFET devices together with the low current and high gain advantage of a cascode configuration to improve the power consumption, gain, noise, and linearity tradeoff in LNA design. Using the newly derived design methodology, we have demonstrated a successful BiFET LNA design. The packaged chip tested on board has achieved a PCS-band gain of 16 dB, a noise figure of 1.6 dB, an IIP3 of -6.5 dBm, and a power consumption of 3 mW. To our knowledge, this is the lowest power consumption reported for an LNA capable of meeting PCS-band requirements.

Appendix

In Fig. 1(d), the voltage gain between V_P and V_{in} can be written as [4]

$$\frac{V_P}{V_{\mathrm{in}}} = -\frac{g_{\mathrm{mBip}}}{g_{\mathrm{mMOS}} + C_P s}. \tag{A.1}$$

Using the Miller rule, we can obtain the equivalent capacitance of C_{BC} from the node P to ground as

$$C_{P\mathrm{BC}} = \left(1 - \frac{V_{\mathrm{in}}}{V_P}\right) \cdot C_{\mathrm{BC}}. \tag{A.2}$$

C_P can be expressed as

$$C_P = C_{\mathrm{GS}} + C_{P\mathrm{BC}}. \tag{A.3}$$

Using (A.1)–(A.3), we can derive C_P as

$$C_P = \frac{(g_{\mathrm{mBip}} + g_{\mathrm{mMOS}})C_{\mathrm{BC}} + g_{\mathrm{mBip}}C_{\mathrm{GS}}}{g_{\mathrm{mBip}} - C_{\mathrm{BC}}s}. \tag{A.4}$$

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Pingxi Ma (M'98) received the Ph.D. degree from Peking University, Beijing, China, in 1994.

In 1997, he was a Visiting Scholar with the Royal Institute of Technology, Stockholm, Sweden. From 1998 to 2000, he was with the University of California at Los Angeles (UCLA) as a Staff Research Associate. He began his industrial career when he joined Conexant Systems and then Jazz Semiconductor Inc., Newport Beach, CA, where he is currently a Senior Designer focused on RF benchmark circuit/circuit intellectual property (IP) design. He has made his main contributions in high-speed polysilicon emitter bipolar devices, GaAs HBTs, and RF circuit design. He has authored and/or coauthored approximately 40 publications in his focused area.

Dr. Ma is a reviewer for the IEEE Transactions on Electronic Device and the IEEE Electronic Device Letters.

Marco Racanelli (S'86–M'91) received the B.S. degree in electrical engineering from Lehigh University, Bethlehem, PA, in 1987, and the M.S. and Ph.D. degrees in electrical engineering from Carnegie–Mellon University, Pittsburgh, PA, in 1989 and 1991, respectively.

He was involved with technology development at Motorola Inc., where he contributed to bipolar, SiGe, and thin-film semiconductor-on-isolator (SOI) development. He then joined Rockwell International, which spun off Conexant Systems and later Jazz Semiconductor Inc., Newport Beach, CA. He has held jobs of increasing responsibility in the area of RF and analog technology development. He is currently the Executive Director of Design Services and Process Engineering for Jazz Semiconductor Inc., where he leads process development, model, design kit, and design support organizations.

Jie Zheng (M'95) received the B.S. degree from Zhejiang University, Hangzhou, China, in 1982, the M.S. degree from Union College, Schenectady, NY, in 1987, and the Ph.D. degree from Arizona State University, Tempe, in 1991, all in electrical engineering.

He was then a Device Model Engineer with Silicon Systems. Since 1996, he has been with Rockwell Semiconductor Systems Inc. (now Jazz Semiconductor Inc.), Newport Beach, CA, where he is responsible for RF device characterization and RF device modeling.

Marion Knight received the B.S. degree in chemical engineering from the University of Illinois at Urbana-Champaign, in 1995.

She is currently a Customer Solutions and Design Automation Engineer with Jazz Semiconductor Inc., Newport Beach, CA.